

20. (Unchanged) The CMOS phase lock loop of claim 15 further comprising means for filtering the error signal from the detecting means before being applied to the tuning means.

21. (Unchanged) The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal, means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.

REMARKS

Claims 1-21 are pending in this application. Claims 22-28 have been canceled without prejudice to prosecute in patent Application No. 09/695,715. Entry of the foregoing amendments is respectfully requested.

Respectfully submitted,

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